	Application No.	Applicant(s)
Notice of Allowability	10/813,595	ZDRAVKOVIC, ANDREJ
	Examiner	Art Unit
	Malcolm D. Cribbs	2115
The MAILING DATE of this communication appl All claims being allowable, PROSECUTION ON THE MERITS IS	ears on the cover sheet with the (OR REMAINS) CLOSED in this	e correspondence address application. If not included
herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT R of the Office or upon petition by the applicant. See 37 CFR 1.313	IGHTS. This application is subject	
1. $igspace$ This communication is responsive to <u>the communication o</u>	on 07/20/06.	
2. ☑ The allowed claim(s) is/are <u>11-37,39-44 and 46</u> .		
3. ☐ Acknowledgment is made of a claim for foreign priority unexpand a) ☐ All b) ☐ Some* c) ☐ None of the:	nder 35 U.S.C. § 119(a)-(d) or (f).	
1. ☐ Certified copies of the priority documents have	e been received.	
2.  Certified copies of the priority documents have	e been received in Application No	. <u></u> .
3.   Copies of the certified copies of the priority do	cuments have been received in the	nis national stage application from the
International Bureau (PCT Rule 17.2(a)).		
* Certified copies not received:		
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONN THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		oly complying with the requirements
4. A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which giv		
5. CORRECTED DRAWINGS ( as "replacement sheets") mus	st be submitted.	
(a) 🔲 including changes required by the Notice of Draftspers	son's Patent Drawing Review ( P1	「O-948) attached
1) 🗌 hereto or 2) 🔲 to Paper No./Mail Date	·	
(b) ☐ including changes required by the attached Examiner Paper No./Mail Date	's Amendment / Comment or in th	e Office action of
Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in t		
<ol> <li>DEPOSIT OF and/or INFORMATION about the deposit attached Examiner's comment regarding REQUIREMENT</li> </ol>		
Attachment(s) 1. ☑ Notice of References Cited (PTO-892)	5. Notice of Informa	al Patent Application (PTO-152)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)	6. 🛛 Interview Summa	ary (PTO-413),
3. Information Disclosure Statements (PTO-1449 or PTO/SB/	Paper No./Mail 08), 7. ⊠ Examiner's Ame	
Paper No./Mail Date  4.  Examiner's Comment Regarding Requirement for Deposit of Biological Material	8.  Examiner's State	ement of Reasons for Allowance
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**EXAMINER'S AMENDMENT** 

An examiner's amendment to the record appears below. Should the changes

and/or additions be unacceptable to applicant, an amendment may be filed as provided

by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be

submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview

with Harry Vartanian on 08/09/2006 at 2:31 PM.

IN THE CLAIMS

**List of Claims:** 

1. (Currently Amended) A method of reducing power consumption of a system

having at least one processor, the processor being coupled to at least one queue which

stores instructions for execution by the processor, the method comprising:

(a) analyzing at least one input;

(b) estimating the a load of the system based, at least in part, on the analysis of

step (a) and by analyzing the a plurality of types of stored instructions in the at least

one queue and assigning a weight to each one of the instructions based on the an

intensity of processing required for each of the instructions;

Application/Control Number: 10/813,595 Page 3

Art Unit: 2115

(c) determining a clock rate based, at least in part, on the estimation of step (b); and

(d) clocking the processor at the clock rate determined in step (c).

19. (Currently Amended) A method of reducing power consumption of a system

having at least one processor, the method comprising:

(a) analyzing at least one input;

(b) estimating a desired processing speed based, at least in part, on the analysis

of step (a) and by analyzing the a plurality of types of stored instructions in at least one

queue coupled to the at least one processor and assigning a weight to each one of the

instructions based on the an intensity of processing required for each one of the

instructions;

(c) determining a clock rate based on the estimation of step (b); and

(d) clocking the processor at the clock rate determined in step (c).

20. (Currently Amended) A method of reducing power consumption of a system

having at least one processor, the method comprising:

(a) analyzing at least one input;

(b) estimating a desired processing rate based, at least in part, on the analysis of

step (a) and by analyzing the a plurality of types of stored instructions in at least one

queue coupled to the at least one processor and assigning a weight to each one of the

instructions based on the an intensity of processing required for each one of the instructions;

21. (Currently Amended) A method of reducing power consumption of a system having at least one processor, the processor being in communication with at least one queue which stores instructions for execution, the method comprising:

controlling the <u>a</u> clocking frequency of the processor in response to a prediction of the <u>a</u> load of the system, the load being based, at least in part, on the instructions stored in the queue and by analyzing the <u>a plurality of</u> types of stored instructions in the at least one queue coupled to the at least one processor and assigning a weight to each one of the instructions based on the <u>an</u> intensity of processing required for each one of the instructions.

- 32. (Currently Amended) A computer system comprising:
  - (a) at least one processor;
  - (b) at least one queue which stores instructions for execution by the processor;
  - (c) a clock electrically coupled to the processor;
- (d) a clock estimation device electrically coupled to the queue and the clock, the clock estimation device being configured to control **the** <u>a</u> frequency of a clock signal output from the clock to the processor; and

wherein the clock estimation device analyzes the <u>a plurality of</u> types of instructions stored in the at least one queue and assigns a weight to each one of the

Application/Control Number: 10/813,595 Page 5

Art Unit: 2115

instructions based on the an intensity of processing required for each one of the

instructions.

41. (Currently Amended) A computer system comprising:

(a) a first processor;

(b) a first load and clock estimation device electrically coupled to the first

processor;

(c) a second processor;

(d) a second load and clock estimation device electrically coupled to the second

processor;

(e) an instruction cache electrically coupled to the first and second processors

and at least one of the first and second load and clock estimation devices, wherein the

first and second load and clock estimation devices are synchronized;

a memory buffer electrically coupled to the instruction cache and the first load

and clock estimation device for queuing all instructions waiting to be executed by at

least one of the processors; and

the first and second load and clock estimation devices analyze the a plurality of

types of instructions stored in the memory buffer and assigns a weight to each one of

the instructions based on the an intensity of processing required for each one of the

instructions.

46. (Currently Amended) A computer system comprising:

(a) an optimum clock estimation device;

(b) at least one long term load estimation device electrically coupled to the

optimum clock estimation device;

(c) at least one short term estimation device electrically coupled to the optimum

clock estimation device;

(d) a clock electrically coupled to the optimum clock estimation device; and

(e) a processor electrically coupled to the clock, wherein each of the long term

and short term load estimation devices analyze a set of instructions, and the optimum

clock estimation device controls the frequency of a clock signal output from the clock to

the processor based on at least one of the long term and short term analysis and a

weight assigned to each one of the instructions in the set of instructions based on the

an intensity of processing required for each one of the instructions.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Malcolm D. Cribbs whose telephone number is 571-272-

5689. The examiner can normally be reached on M-F 8AM-430PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number: 10/813,595 Page 7

Art Unit: 2115

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Malcolm D Cribbs Examiner Art Unit 2115

August 10, 2006

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